REMARKS/ARGUMENTS

In the specification, the paragraphs [0068], [0077], and [0085] have been amended to include reference to the now available U.S. Patent number which resulted from U.S. application Ser. No. 09/291,315, which had been expressly incorporated by reference in its entirety into the present application. The corresponding U.S. Patent issued shortly after the present application was filed with the U.S. Patent Office. In addition, the paragraphs [0039], [0084], [0085], and [0086] have been amended to correct and clarify references to certain element numerals in the drawings. The paragraphs [0064] and [0082] of the specification have been amended to correctly refer to N_r and $N_{y'}$, the number of pixels in the frame buffer in the r-dimension and in the y'-dimension, respectively, rather than N_x and N_y, in accordance with the standard transformation from Cartesian coordinate system to cylindrical coordinate system. It is respectfully submitted that no new matter has been introduced into the present application by this Amendment.

Upon entry of this Amendment, Claims 1, 2, 4-9, 12, 13, 16-23, 47, 48, 50-55, 58, 59, and 62-91 will remain pending in this application. Claims 1, 2, 4-9, 12, 13, 16, 17, 20-23, 47, 48, 50-55, 58, 59, and 62-69 have been amended, Claims 3, 10, 11, 14, 15,

24-46, 49, 56, 57, 60, and 61 have been canceled, and Claims 70-91 have been added by this Amendment. Reconsideration and allowance of all of the pending claims in view of the foregoing amendments and the following remarks are respectfully requested.

In Claims 47, 48, 50, 52, 54, 55, 58, 62, and 66-69, Applicants have amended the term "microprocessor" to "graphics data processor," as Applicants believe that the microprocessor limitation unduly narrows the scope of the claimed invention as disclosed in, *inter alia*, paragraphs [0036]-[0039] and [0049]-[0052] in the specification. For example, paragraph [0037] of the specification discloses that "[v]ideo controller 105 . . . can be ***any suitable hardware, software, or any combination thereof capable of performing suitable graphical manipulations***." (emphasis added). In addition, paragraph [0052] of the specification discloses the following:

> Video circuitry 410 may include any suitable circuitry for managing or manipulating data received from graphics source 110 and for transmitting the data to frame buffer 420. Video circuitry 410, for example, may be suitable proprietary hardware, or may be any suitable commercially available GPU [graphics processing unit]. It may be a graphics application program of a computer that operates an API, or any other suitable hardware, software, or combination thereof.

In all of the claims having the "frame buffer" limitation, Applicants have amended the term "frame buffer" to "multiplanar frame buffer" to further clarify and emphasize

that the frame buffer in the claimed invention differs from a conventional frame buffer for displaying images on a two-dimensional display. As stated in paragraph [0010] of the specification, "conventional frame buffers are inadequate because they lack the capacity and data organization to store (x,y,z) coordinate image data such that satisfactory three-dimensional images can be displayed." Hence, as stated in following paragraph [0011] of the specification, one of the objectives of the present invention is "to provide a frame buffer that has the capacity to store and quickly transfer image data organized such that satisfactory three-dimensional images can be displayed," *i.e.*, a multiplanar frame buffer. Examples of multiplanar frame buffers in some embodiments of the present invention are disclosed in, *inter alia*, paragraphs [0053]-[0073] and [0080]-[0091] of the specification. Applicants respectfully note that, as is clear from the above-cited portions of the specification, the adjective "multiplanar" in the multiplanar frame buffer in no way indicates any specific physical or logical structure of the frame buffer memory, but is only meant to distinguish the frame buffer of the present invention from the conventional frame buffer for a two-dimensional display system.

Claims 8 and 54 have been amended to correctly refer to N_r and $N_{y'}$, the number of pixels in the frame buffer in the r-dimension and in the y'-dimension, respectively,

rather than N_x and N_y, in accordance with the standard transformation from Cartesian coordinate system to cylindrical coordinate system.

Applicants have added new Claims 70-75 to more clearly capture Applicants' inventions disclosed in, *inter alia*, paragraphs [0084] and [0086] of the specification and FIG. 5d; Claims 76-79 to more clearly capture Applicants' inventions disclosed in, *inter alia,* paragraphs [0054] and [0080] of the specification and FIGS. 4b and 4c; Claims 80 and 81 to more clearly capture Applicants' inventions disclosed in, *inter alia*, paragraph [0070] of the specification and FIGS. 6a-6c; Claims 82 and 83 to more clearly capture Applicants' inventions disclosed in, *inter alia*, paragraph [0089] of the specification and FIG. 6d; and Claims 84-91 to more clearly capture Applicants' inventions disclosed in, *inter alia*, paragraphs [0080]-[0086] of the specification and FIG. 5d of the present application.

Claim Rejections - 35 U.S.C. § 102

We now address the Examiner's prior art rejection, which we respectfully traverse. In the July 2, 2003 Office Action, the Examiner has acknowledged that Claims 6, 8, 29, 31, 52 and 54 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, the Examiner

rejected remaining Claims 1-5, 7, 9-28, 30, 32-51, 53 and 55-69 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,706,816 to Mochizuki et al. ("the '816 Patent"). Applicants respectfully submit that none of the pending claims in the present application as amended is anticipated by the '816 Patent as the '816 Patent does not disclose, either expressly or inherently, a multiplanar frame buffer and a three-dimensional display for displaying three-dimensional images.

The '816 Patent is directed to a method and apparatus for generating images based on ultrasound echoes from a three-dimensional object. *See* the '816 Patent, at Col. 1, lines 13-18. However, the '816 Patent only discloses methods and means of performing such methods to display images on a two-dimensional display system that are perceived to be three dimensional on the same basis that a television image is perceived to be "three dimensional," rather than true three dimensional images occupying a definite volume of three-dimensional space as shown in the present invention.

More specifically, element 42 in FIG. 1 shows a display for displaying a ultrasound image. The '816 Patent teaches that a CRT (cathode-ray tube) can be used for such display. *See* the '816 Patent, at Col. 9, line 20. As is well known, a CRT is a conventional two-dimensional display used in televisions and computer displays. In fact,

FIG. 4 of the '816 Patent shows how the ultrasound image data is projected onto a two-dimensional display screen. The '816 Patent teaches:

> A value obtained by processing a number of voxels[2] of an ultrasound beam sequentially from the first (initial) voxel 20 corresponds to ***a brightness value P(x,y) of one [1] pixel in the ultrasound image 100 on a display screen***.

The '816 Patent, at Col. 11, lines 52-56 (emphasis added); *see also id.* at Col. 8, lines 51-53. Since each pixel of the display is only assigned with x and y coordinate information, this clearly indicates that the '816 Patent is only directed to a method and apparatus of displaying ultrasound images on a conventional two-dimensional display system. Nowhere in the '816 Patent is there any disclosure or even suggestion of displaying ultrasound image on a truly three-dimensional volumetric display system.

Neither does the '816 Patent disclose a multiplanar frame buffer for a three-dimensional display system, which maintains scaled z-coordinate information as well as x and y coordinate information for each pixel. As the method and apparatus disclosed in the '816 Patent only use a conventional two-dimensional display system such as CRT, the '816 Patent merely discloses a conventional x-y frame buffer (or "frame memory") for such two-dimensional display system:

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[2] In the '816 Patent, voxel is defined as a sampling point of ultrasound echo data in a ultrasound beam direction and is not an element of the image display means. *See* the '816 Patent, at Col. 11, lines 33-48.

> [T]his frame memory has ***X-Y addresses corresponding to the pixels of a display screen*** for displaying an ultrasound image on a one-to-one basis. . . . [T]he brightness value data for the respective ultrasound beams are written into corresponding predetermined X-Y addresses in the frame memory, respectively.

The '816 Patent, at Col. 8, line 66--Col. 9, line 16 (emphasis added). Nowhere in the '816 Patent is there any disclosure or even suggestion of using a non-conventional multiplanar frame buffer for a three-dimensional display system.

On the other hand, the present invention is directed to generation of three-dimensional images using a truly three-dimensional volumetric display such as a multiplanar volumetric display system in which the images occupy a definite volume of three-dimensional space and are projected onto multiple display elements arranged in the depth direction. Thus, all of the independent claims of the present application (*i.e.*, Claims 1, 24 and 47) as amended herein require a frame buffer for displaying three-dimensional images on a three-dimensional display, *i.e.*, a multiplanar frame buffer. Unlike the conventional frame buffer used in the '816 Patent, a memory location in a multiplanar frame buffer of the present invention is associated with each pixel of the three-dimensional display based not only on the pixel's x- and y-coordinate information, but also on its scaled z-coordinate information. *See, e.g.*, par. [0014] of the specification of the present application.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently, in a single prior art reference. *See* MPEP 2131. Since the '816 Patent does not disclose, either expressly or inherently, a multiplanar frame buffer for use with a three-dimensional display system, Applicants respectfully submit that the '816 Patent cannot anticipate independent Claims 1, 24 and 47 of the present application. Since none of the independent claims pending in the present application cannot be anticipated by the '816 Patent, none of their respective dependent claims incorporating all of their elements cannot be anticipated by the '816 Patent either.

Accordingly, Applicants respectfully submit that the '816 Patent does not anticipate any of the pending claims in the present application as amended. It is respectfully requested that this rejection be withdrawn and that all of the pending claims be allowed over the '816 Patent.

In light of the foregoing amendments and remarks, Applicants respectfully request that the rejection be withdrawn and that a timely Notice of Allowance with respect to all of the pending claims be issued in this case.

Included herewith is a petition for a three-month extension of time. A check in the amount of $475.00 is also included herewith to cover the fee for a three month extension of time for response for a small entity. No additional fees or extensions of time are believed to be due. However, authorization is given hereby to charge Deposit Account No. 01-1785 for any deficiency in fees necessary to preserve the pendency of the subject application, or to credit the same in case of overpayment.

Respectfully submitted,

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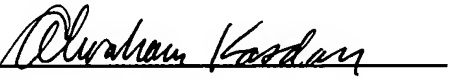
By: 
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